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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/780,513	02/17/2004	Bor-Wen Chan	TS03-485	1381
42717	7590	06/29/2005	EXAMINER	
HAYNES AND BOONE, LLP 901 MAIN STREET, SUITE 3100 DALLAS, TX 75202			MITCHELL, JAMES M	
			ART UNIT	PAPER NUMBER
			2813	

DATE MAILED: 06/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No. 10/780,513	Applicant(s) CHAN ET AL	
	Examiner James M. Mitchell	Art Unit 2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 20 April 2005.  
 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.  
 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-25 is/are pending in the application.  
 4a) Of the above claim(s) 21-25 is/are withdrawn from consideration.  
 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.  
 6) ☒ Claim(s) 1-20 is/are rejected.  
 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.  
 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.  
 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) ☐ All b) ☐ Some \* c) ☐ None of:  
 1. ☐ Certified copies of the priority documents have been received.  
 2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
 \* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>4/15/04</u> . | 6) <input type="checkbox"/> Other: _____  |

### **DETAILED ACTION**

1. This office action is in response to applicant's election filed April 20, 2005.

#### ***Election/Restrictions***

2. Claims 21-25 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Applicant's election without traverse of claims 1-20 in the reply filed on April 20 is acknowledged.

#### ***Drawings***

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the sidewalls having a first and second thickness must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.
4. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an

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application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

***Claim Rejections - 35 USC § 112***

5. Claims 9 and 12-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.
6. With respect to claim 9, the antecedent basis in claim 1 for the dielectric having a first and second thickness in claim 1 is the sidewalls (i.e. spacers formed on polysilicon). Yet applicant's written specification (Page 8, 9) indicates that the dielectric layer that has a first and second thickness is the gate oxide layer; no reference is made to varying thickness of sidewall spacers.
7. With respect to claim 12, line 4, there is no antecedent basis for "said dielectric".

***Claim Rejections - 35 USC § 102***

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States

only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. Claims 1, 4, 5, 10, 11 are rejected under 35 U.S.C. 102(e) as being anticipated by Kasuya (U.S. 6,753,215).

10. Kasuya (Fig.2a-5b, 8a,b) discloses:

(cl. 1) a method to form metal silicide gates in the fabrication of an integrated circuit device, said method comprising: forming polysilicon lines (32) overlying a substrate (10) wherein said polysilicon lines have dielectric sidewalls (62); forming a first isolation layer overlying (50) said substrate and said dielectric sidewalls wherein said first isolation layer does not overlie the top surface of said polysilicon lines (Fig. 3b); partially etching down said polysilicon lines such that said top surfaces of said polysilicon lines are below the top surface of said dielectric sidewalls (Fig. 4a); thereafter depositing a metal layer (36) overlying said polysilicon lines; thermally annealing (Col. 11-12, Lines 66-3) to completely convert said polysilicon lines to metal silicide gates; and removing unreacted said metal layer (Fig. 8b) to complete said device;

(cl. 4) forming a first isolation layer further comprises: depositing an interlevel dielectric layer (i.e. lower layer of multilayer, 50; Fig. 1) overlying said substrate and said polysilicon lines; and planarizing (Col. 8, Lines 53-54) said interlevel dielectric layer;

(cl. 5) implanting ions into said substrate (42; Col. 8, Lines 34-36) prior to said step of forming a first isolation layer (Fig. 2a-3a) to thereby form first doped regions in said substrate and adjacent to said polysilicon lines;

(cl. 10) and the step of partially etching down said polysilicon lines results in a thickness of polysilicon lines of 100 to about 500 Å (Col. 8, Lines 10-11, 59-61);

(cl. 11) wherein said metal silicide gates have a thickness of between about 180 Å and about 900 Å (i.e. silicide is made from metal; Col. 11, Lines 61-62);

***Claim Rejections - 35 USC § 103***

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

12. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kasuya (U.S. 6,753,215).

13. Kasuya discloses the elements stated in paragraph 10 of this office action, but does not show first and second thickness of dielectric sidewalls that are not equal, or that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical.

14. In any case, the dimensions would have been obvious, since it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, *In re Rose*, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); *In re Rinehart*, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); *Gardner v. TEC Systems, Inc.*, 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); *In re Dailey*, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

15. Claims 2, 3 and 6-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kasuya (U.S. 6,753,215) as applied to claim 1 and further in combination with Xiang (U.S. 2005/0054164).

16. Kasuya further discloses forming spacers (62) with a thickness prior to step of partially etching polysilicon lines, implanting ions into said substrate to thereby form second doped regions (44) and depositing a second metal (36), but does not explicitly disclose the use of etching back a spacer layer to form spacer or covering polysilicon with a hardmask for patterning of gates.

17. Xing shows etching back a spacer layer to form sidewall spacers and covering polysilicon with a hardmask for patterning of gates (Par. 0032, 0037).

18. It would have been obvious to one of ordinary skill in the art to incorporate a step of etching back a spacer layer in Kasuya and forming a hardmask over the polysilicon lines of Kasuya prior to partially etching down the lines, in order to form the sidewalls spacers by a known method and to pattern gates as required by Kasuya (Col. 8, Lines 18-20 & 9-10,) such that the hard mask use would be done prior to etching down step (i.e. etching down step is done after formation of gate, Fig. 4a).

19. With respect to the claimed thickness in claim 8, applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See paragraph 14 of this office action.

20. Claims 12-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kasuya (U.S. 6,753,215) in combination with Xiang (U.S. 2005/0054164).

21. Kasuya discloses the elements stated in paragraph 10 of this office action and further said polysilicon overlying a dielectric layer (20), implanting ions into said substrate to thereby form a second doped regions (44) and depositing a second metal (36), but does not explicitly disclose the use of etching back a spacer layer to form spacer or covering polysilicon with a hardmask for patterning of gates.

22. However, see paragraphs 17-19 of this office action.

23. With respect to the claim thickness of claim 18, since applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical (Appl. Spec. Page 9, Line 1-2). See paragraph 14 of this office action.

### ***Conclusion***

24. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The prior art discloses in: Lee (U.S. 2005/0118531) the use of a hard mask overlying the polysilicon layer, patterning mask and then patterning polysilicon.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James M. Mitchell whose telephone number is (571) 272-1931. The examiner can normally be reached on M-F 8:00-4:00.



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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jmm  
June 16, 2005

